STATEMENT OF WORK

1. **Objective/Requirements**
    a. The objective of this work is to design and fabricate silicon CMOS pixel detectors for the AstroPix ISFM. The sensors designed by the contractor and manufactured at a silicon CMOS foundry are prototypes used by NASA GSFC for internal scientific purposes and demonstration of capabilities. This is broken into 3 separate parts:
        i. The first objective is to design and fabricate a small test chip at a silicon CMOS foundry
        ii. The second objective will be to develop a test system for the sensors to characterize the first iteration of these detectors
        iii. The third objective will be to design and fabricate a full chip based on a validate design (second iteration of these detectors)
    b. The requirements are below:
        i. **Supplies:**
            1. Analog Supply VDDA: 1.8V
            2. Analog Supply VSSA: 1.2V
            3. Digital Supply VDDD: 1.8V
            4. Analog Ground GNDA
            5. Digital Ground GNDD
            6. Sensor Reverse Bias Voltage: 0 to 400V
            7. External Bias: Possible for all 4 voltages
        ii. **Pixel Matrix:**
            1. 36 cols x 34 rows - 1224Pixels
            2. 500u Pixel Pitch and 300u Pixel Size
            3. 3 Tune bits per Pixel
            4. Pixel Dynamic Range 20keV - 700keV
            5. Noise Floor 5keV (2%@662keV)
            6. Bias Voltage up to 400-500V to maximize depletion
            7. In Pixel amplifier with Dynamic Feedback option for improved Dynamic Range
        iii. **Matrix Digitization:**
            1. 1 Hit buffer per Pixel
            2. Each Column has an “End-of-Column” buffer
            3. Timestamps for both edges:
                a. 15 bit@2.5 MHz
                b. 3 bit@20MHz
            4. 16-bit Flash-TDC
        iv. **Periphery:**
            1. 6x10b VDAC
            2. Integrated injection switch (with VDAC)
            3. 2 temperature sensors without ADC and buffer
            4. PLL 20 MHz from 2.5 MHz Ref Clk
            5. DLL for TDC stabilization
        v. **Power dissipation:**

1. Target at < 1.5mW/cm2

vi. **Digital Interface:**

1. 2 SR Interfaces (General, TDAC)
2. TS Clock: 2.5Mhz (Latency only important for Timing, Jitter must be low)
3. LVDS 20 MHz clock (backup if PLL does not work) (Internal termination and power down can be configured vi SR)
4. Common Interrupt for row wake-up
5. Common Hold for data discarding
6. Unique ID for each APS
7. 5 QSPI I/O: Quad SPI in Daisy Chain
    a. CLK 20 Mhz: Chip-to-Chip
    b. MOSI: Chip to Chip (Left to right in the chain)
    c. MISO [1:0]: Chip to Chip (right to left in the chain)
    d. CS (Chips Select): right to left to synchronize Chip output and input stages

2. Characteristics, Scope, and Specs

a. Characteristics:
    i. The chips will have a dynamic range of 20 keV – 700 keV, a noise floor of 5 keV, an energy resolution of 10% at 120 keV, and a target power consumption of 1mW/cm2.

b. Scope:
    i. HVCMOS silicon pixel detectors with 500 x 500 um pixel pitch
    ii. Each pixel will contain an NMOS amplifier and an isolated PMOS comparator
    iii. Signal injection for compatibility testing

c. Specs:
    i. Multiple resistivities to confirm depletion, these can be determined by the capabilities of the foundry but must have at least 3kOhm-cm resistivity.

3. Place of Performance

a. The work shall be performed at the contractor's facility, or a subcontracted facility as determined by the contractor

4. Period of Performance

a. Work will be performed nominally between July 1, 2026 and July 1, 2028. The exact dates are to be agreed upon as the project progresses,